Development of Three-Dimensional Inductors Using Plastic Deformation Magnetic Assembly (PDMA)

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***Abstract*—On-chip inductors are critical for enabling portable power-efficient wireless communication systems. Existing on-chip spiral inductors based on conventional planar integrated-circuit fabrication technology suffer from substrate loss and parasitics, and have relatively large footprints. In this paper, we discuss the development of two types of on-chip three-dimensional (3-D) inductors—a vertical spiral inductor and a solenoid inductor—by using a 3-D assembly process called plastic deformation magnetic assembly. Prototype vertical spiral inductors and solenoid inductors have been fabricated and tested. Experimental results show that the vertical spiral inductors can achieve better performance and a smaller footprint than the in-plane ones.**

***Index Terms*—On-chip solenoid inductor, plastic deformation magnetic assembly (PDMA), three-dimensional (3-D) assembly, vertical spiral inductor.**

I. Introduction

HIGH-PERFORMANCE on-chip inductors are critical for enabling integrated wireless communication systems. Planar spiral inductors that lie in the substrate plane are widely used in radio-frequency integrated circuits (RFICs). However, such in-plane inductors involve substrate loss and parasitics (especially on silicon substrate) [1], [2]. As a result, their quality factor and self-resonance frequency are generally low. Oftentimes, discrete inductors with better performances have to be used to meet the system performance requirement. However, the use of discrete components introduces parasitics (associated with wire leads), making the system integration and miniaturization more difficult. Also, conventional spiral inductors usually have relatively large footprints, which decreases the potential density of integration and is especially undesirable when the inductors are made on costly III–V compound semiconductor substrates.

Direct monolithic integration of high-performance inductors with integrated circuit (IC) elements provides several advantages. First, smaller parasitics can be achieved due to shorter interconnects. Second, it could potentially make wireless communication devices more compact and reliable. Third, it would reduce the fabrication costs of RF microsystems by eliminating assembly steps encountered in the multichip-module approach.

In recent years, much effort has been made to improve the performance of on-chip spiral inductors. A common theme of research is aimed at increasing the quality factor by reducing losses associated with substrate leakage and decreasing the coil resistance. Certainly, the performance can be improved by using low-loss materials and substrates such as gallium arsenide [3]–[5]. However, silicon substrates are of low costs and, therefore, prove to be attractive to commercial RFIC development. Published research work for improving the performance of inductors on silicon substrates generally fall into two major categories: 1) applying micromachining technologies to separate the inductors from the substrates [6]–[13] and 2) using a post-fabrication assembly processes to tilt the inductor away from the substrate surface [14], [15].

It is important to note that an optimal inductor solution would need to provide not only good performance, but also compatibility with the industrial-standard foundry process. In this regard, micromachining steps such as bulk etching and the use of thick sacrificial layers tend to introduce issues of compatibility with existing foundry processes. Also, the large footprints issue of the inductor is still not solved.

In our opinion, the second approach is more promising, which could result in both improved performance and reduced footprints. We believe that such a process is more likely to be accepted by the IC foundry because the process can be appended to existing process flow and the inductor can be added to existing IC chips as superstructures.

II. Design Concept

A. Plastic Deformation Magnetic Assembly (PDMA) Process

Inductors with spiral coils that are lifted out of the substrate plane have been reported [14], [15]. The assembly process proposed in [14] is reported to work with thin metal structures. This may limit its use in assembling spiral inductors with thick metal films (e.g., several micrometers of thickness) for the purpose of reducing series resistance. The assembly process reported in [15] relies on the phase change of manually placed solder spheres. This process requires individual deployment of small solder spheres on the substrate and, thus, is not suitable for mass production.

We have developed a new three-dimensional (3-D) microstructure assembly process called PDMA. Using the PDMA

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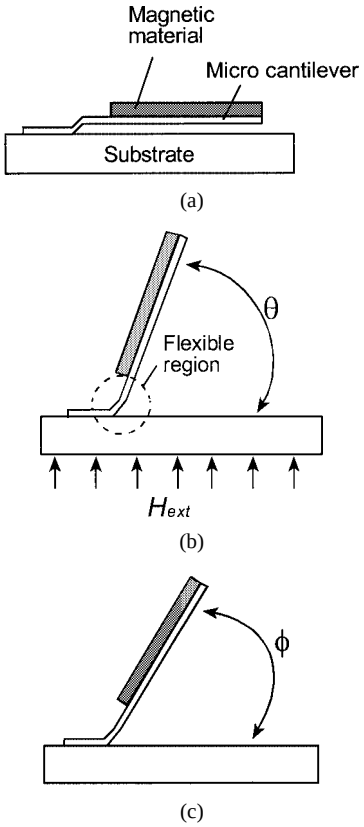


Fig. 1. Schematic diagram of the PDMA process.

process, surface micromachined structures can be bent out of the substrate plane permanently and maintain their profile without outside energy or force input. In our opinion, this technique offers two important advantages. First, the process is simple and involves only three layers of thin films (two structural layers and one sacrificial layer). Secondly, the fabrication process is efficient and can be conducted in parallel at wafer scale.

The development of the PDMA process has been discussed in [16]. Since this paper focuses on discussing applications enabled by the PDMA process, it is necessary to briefly describe its basic concept (Fig. 1). For simplicity, we use a surface micromachined cantilever as an example. First, a surface-micromachined cantilever is fabricated on top of a substrate, with one end directly anchored to the substrate and the remaining portion lying on a sacrificial spacer. The cantilever is made of ductile metals such as gold, aluminum, or copper. These materials have relatively low yielding strength and, hence, can be plastically bent more easily compared with other metal materials. Since the cantilever is made of metal, electrical leads between the lifted structure and substrate surface can be easily established.

A piece of magnetic material is then attached to the cantilever. For example, a ferromagnetic material, permalloy $(Ni_{80}Fe_{20})$, can be electroplated onto the cantilever. Areas of the cantilever that is covered by the magnetic material is generally much stiffer compared to areas that are not covered. Specifically, a segment of the cantilever between the anchor and one end of the magnetic piece (closest to the anchor) is thin and can bend under an applied moment.

Next, the cantilever is "released" from the substrate by removing the sacrificial layer [see Fig. 1(a)]. If an external magnetic field (with a field intensity denoted as H_{ext}) is applied from underneath the substrate, the magnetic piece on the cantilever will be magnetized in the applied magnetic field. As a result, the torque generated in the magnetic material piece will bend the cantilever off the substrate [see Fig. 1(b)]. The bending angle of the cantilever θ increases with the magnitude of H_{ext}. When the bending angle reaches a certain threshold, the bending region will encounter irreversible plastic deformation as the internal stress exceeds the yield strength of the cantilever material. After the magnetic field is removed, the cantilever will remain at a certain rest angle ϕ off the substrate [see Fig. 1(c)]. The angle ϕ may be smaller than the maximum value of θ. However, the difference may be quite small. Details of the mechanical modeling and design rules for the PDMA process can be found in [16].

B. Vertical Spiral Inductors

Fig. 2 illustrates the general concept of developing on-chip vertical spiral inductors using the PDMA process. The starting substrate may contain IC elements such as resistors, diodes, or transistors [see Fig. 2(a)]. An in-plane spiral inductor is then fabricated on the substrate [see Fig. 2(b)]. The spiral inductor consists of two metal layers and one dielectric layer. The first metal layer forms the coil. The second metal layer connects the inner end of the spiral coil to an anchor outside the periphery of the coil to complete the coil continuity. A dielectric layer prevents the second-layer metal from contacting the first-layer metal. The spiral coil lies on top of a patch of sacrificial material. Magnetic materials can be placed on top of the planar coil by overlapping with the coil patterns made in the first metal layer. It may be possible to have the in-plane inductor to overlap with circuit elements to maximize the efficiency of chip space.

After the sacrificial layer is removed to free the planar coil, the spiral inductors are assembled to their vertical position using the PDMA process [see Fig. 2(c)]. The vertical planar spiral inductors are designed as a one-port coplanar waveguide (CPW) configuration with three test pads to facilitate testing with Cascade on-wafer probes and network analyzers.

Since the vertical spiral inductors are raised away from the substrate, the substrate loss, parasitics, and also the footprints of the inductors are reduced. The coupling between vertical inductors and the substrate is generally much less than that of the in-plane ones. Thus, the vertical inductors can be initially patterned over circuit elements, essentially increasing the potential density of integration. Moreover, this PDMA-based process provides unique advantages over the aforementioned lifting processes. Spiral inductors with either thin or thick metallization can be assembled. The rotation angle of the inductor can be adjusted during the assembly. No additional supporting structures are needed to hold the vertical inductors after the assembly.

C. On-Chip Solenoid Inductors

Besides spiral inductors, solenoid inductors can also be useful in RFICs. Several research papers on on-chip solenoid inductors have been reported [17]–[19]. In [17], an alumina core is manually placed onto the substrate and copper windings are directly deposited around the core using a mould formed by 3-D laser photolithography. In [18] and [19], multiple layers of electroplated metals are used to make the 3-D solenoid structures. The

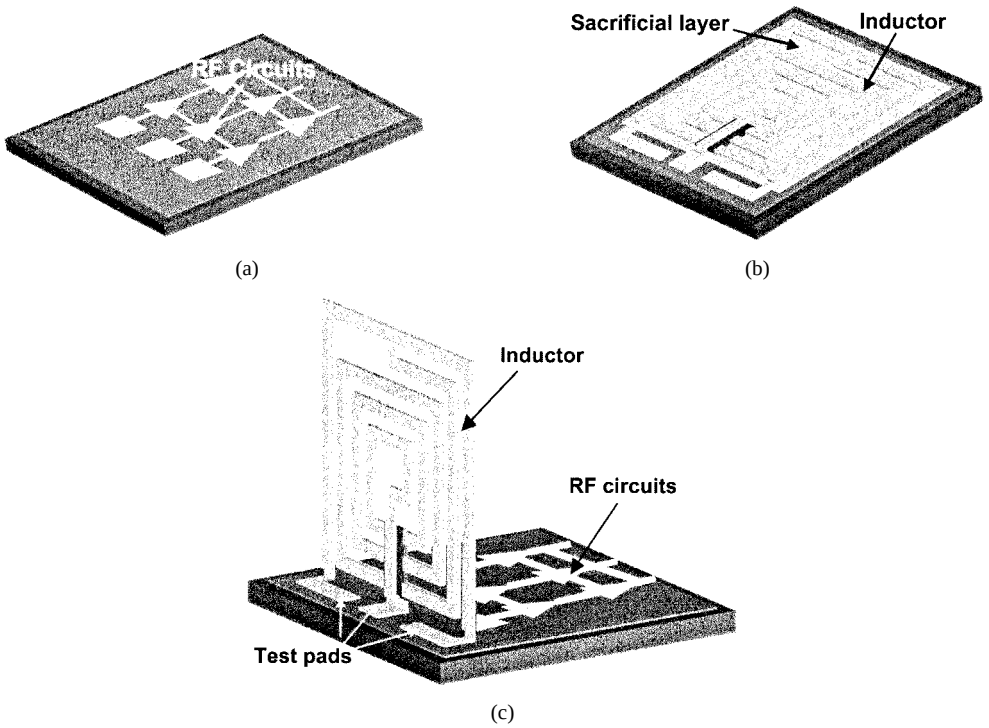


Fig. 2. Schematic diagram of building a vertical spiral inductor using the PDMA process.

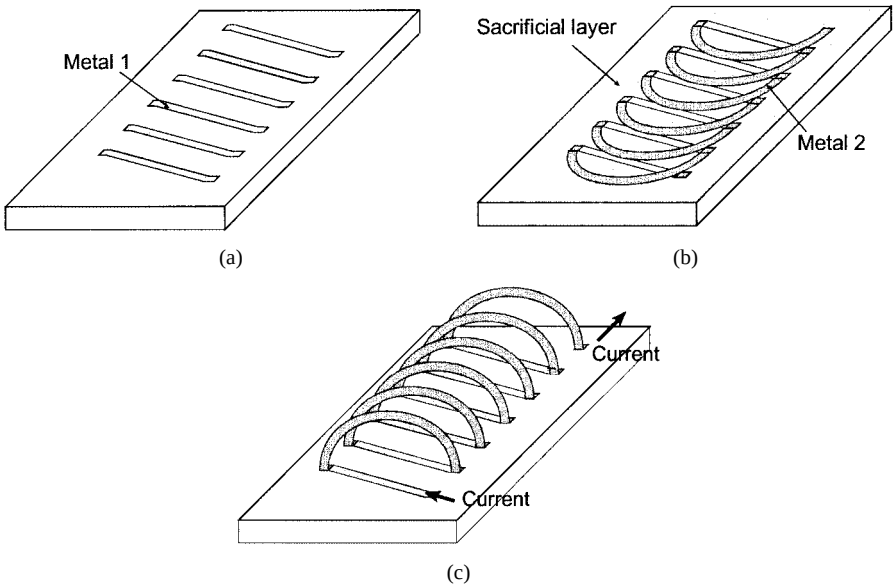


Fig. 3. Schematic diagram illustrating the concept of on-chip solenoid inductor development using the PDMA process.

cross-sectional area of the on-chip solenoid inductor depends on the height of the electroplated posts.

In this paper, we present an alternative method to form on-chip solenoid inductors with nearly arbitrary cross-sectional shapes and dimensions (Fig. 3). Different from the processes discussed above, the 3-D winding structures are not made by direct 3-D construction, but by the assembly of two-dimensional (2-D) multilayer structures. First, a metal layer (Metal 1) is deposited onto the substrate and patterned [see Fig. 3(a)]. Multiple parallel metal traces are formed. Second, a second metal layer (Metal 2) is deposited and patterned to form curved wire leads [see Fig. 3(b)]. The two metal layers are separated by a sacrificial layer between and connected only at via-holes, which are located at the ends of the parallel lines in Metal 1. Magnetic material is then electroplated to overlap with Metal-2 patterns. Next, the sacrificial layer is removed and the PDMA process is used to assemble the top-level winding structures (Metal 2) into vertical position to form a 3-D solenoid inductor [see Fig. 3(c)].

This method allows two unique capabilities. First, solenoid with arbitrary cross section can be realized. Secondly, relatively large volume of solenoid can be fabricated by incorporating metal thin films. Magnetic cores are currently not integrated with the prototype solenoid inductors.

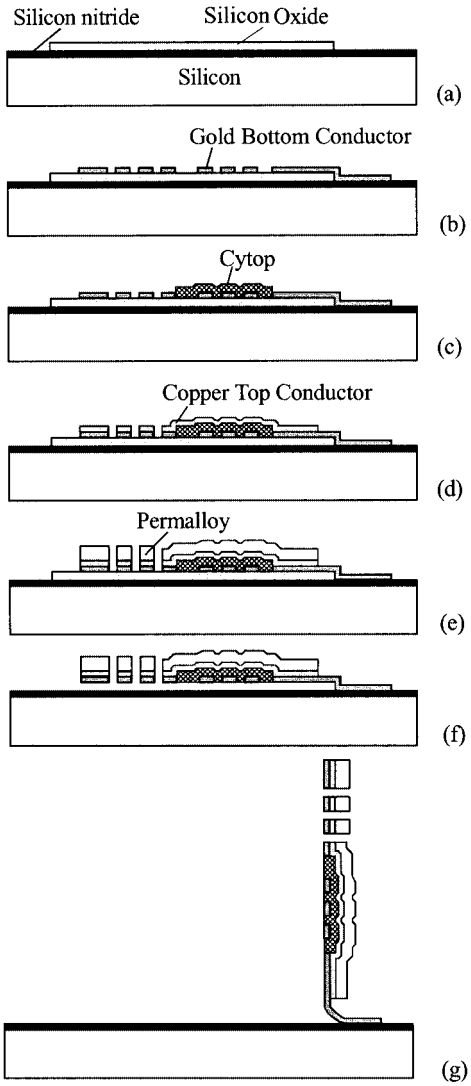


Fig. 4. Schematic diagram of the fabrication process of the first-generation on-chip vertical spiral inductor.

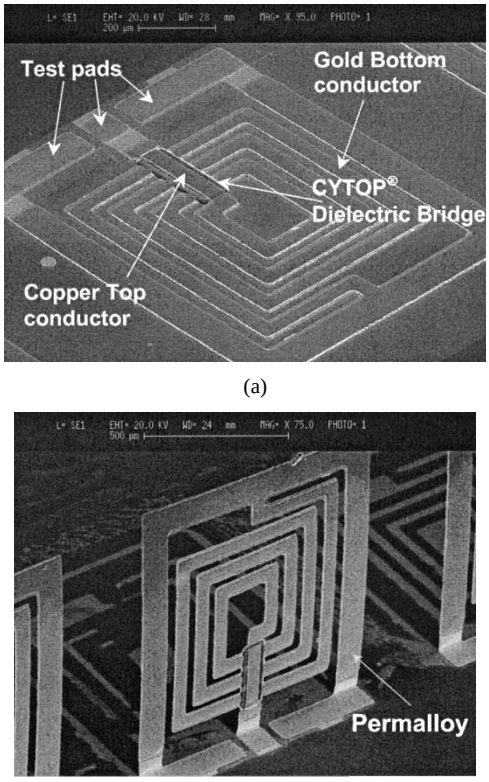


Fig. 5. Scanning electron micrographs of a 4.5-nH first-generation on-chip spiral inductor. (a) Spiral inductor lies in the substrate plane before the PDMA assembly. (b) Inductor stands above the substrate after the PDMA assembly.

III. Development of On-Chip Vertical Spiral Inductors

Thus far, the development of on-chip vertical spiral inductors consists of two phases. In the first phase, we aimed to demonstrate the proof-of-concept prototype. Some results have been previously reported in [16] and [20]. In the second phase, we improved the design and fabrication process to achieve higher quality factor.

A. First-Generation On-Chip Vertical Spiral Inductors

The fabrication process of the first-generation on-chip vertical spiral inductors is shown in Fig. 4. The inductors are fabricated on a silicon substrate coated with a 0.6-μm-thick silicon nitride layer serving as dielectric insulation. However, this process also allows inductors fabrication directly on glass or polymer substrates.

First, a 0.5-μm-thick silicon oxide layer is deposited and patterned to serve as the sacrificial layer [see Fig. 4(a)]. A 0.5-μm -thick gold layer is deposited onto the substrate and patterned to make the spiral coil of the inductor [see Fig. 4(b)]. Part of the coil conductor overlaps with the sacrificial layer, while the remainder of the coil conductor deposited directly on the substrate, forming a solid anchor. Subsequently, a 2.5-μm-thick CYTOP film (CYTOP-809M, Asahi Glass Corporation, Tokyo, Japan) is spun onto the gold layer and patterned as the dielectric spacer [see Fig. 4(c)]. A 1.5-μm-thick copper layer is deposited and patterned to make the top conductor used to complete the spiral coil [see Fig. 4(d)]. A 5-μm-thick permalloy layer is electroplated onto the copper and gold surfaces. The permalloy film increases the stiffness of the coil [see Fig. 4(e)]. After the oxide sacrificial layer is etched and the inductor structure is released from the substrate [see Fig. 4(f)], the entire inductor structure is assembled into vertical position using the PDMA process [see Fig. 4(g)]. Fig. 5 shows a first-generation 4.5-nH vertical spiral inductor fabricated using the process discussed above.

The S_{11}-parameter of the inductors is measured from 50 MHz to 4 GHz using an HP 8510C network analyzer and a Cascade coplanar GSG-150 probe. The one-port short–open–load calibration technique is used. The performance of the inductor is also estimated using a comprehensive simulation tool (ADS, Agilent Technologies, Santa Rosa, CA). Fig. 6 shows the simulated and measured S_{11}-parameter results of the spiral inductor shown in Fig. 5 before and after the PDMA assembly. The effects of the probing pads that feed the inductors are deembedded. The extracted quality factor Q as a function of frequency is shown in Fig. 7. The Q factor is estimated by using the following procedure. First, we experimentally measure the S_{11}-parameter of the spiral inductor (including the feeding pads) and that of a test structure with only the feeding pads. Second, the one-port impedance of the inductor is calculated from the deembedded

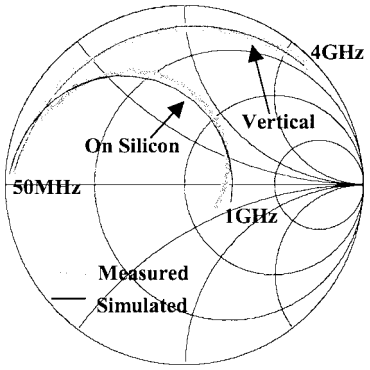


Fig. 6. Simulated versus measured S_{11}-parameter of the spiral inductor before and after the PDMA assembly.

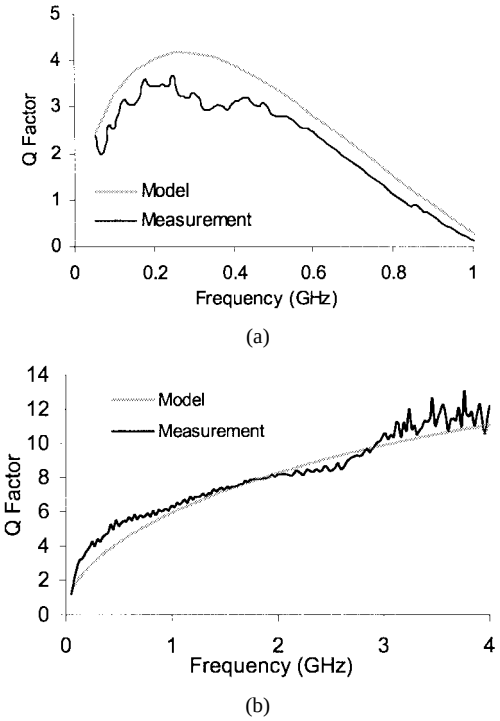


Fig. 7. Quality factor Q of the spiral inductor extracted from the simulated and measured S_{11}-parameters. (a) Before the PDMA assembly. (b) After the PDMA assembly.

S_{11}-parameter. The Q factor is estimated by dividing the imaginary part of the impedance (reactance) with the real part of the impedance (resistance). When the spiral inductor is lying within the substrate plane, it has a peak quality factor of 3.5 and its self-resonance frequency is approximately 1 GHz. After the PDMA assembly, the same inductor exhibits a peak quality factor of 12 and a self-resonance frequency of well above 4 GHz.

B. Second-Generation On-Chip Vertical Spiral Inductors

In the development of the second-generation on-chip vertical spiral inductors, several modifications were made in the first-phase process to improve the inductor's quality factor.

First, in order to reduce the series resistance of the inductor, the spiral coil of the second-generation inductor is made of a 10-μm-thick copper layer instead of the 1.5-μm-thick layer used in the first generation. An electroplating process is used to realize thick copper layers due to its much higher deposition rate than evaporation.

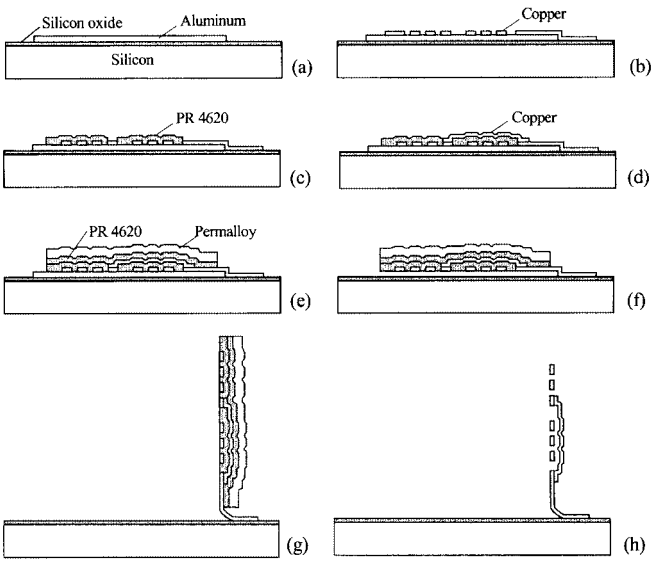


Fig. 8. Schematic diagram of the fabrication process of the second-generation vertical spiral inductor.

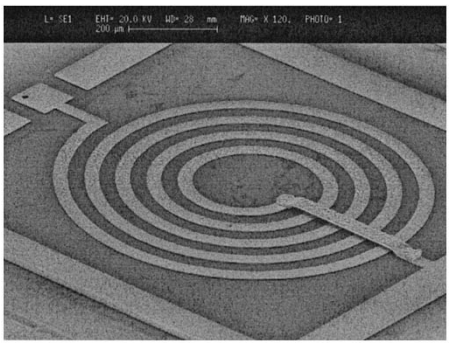
Second, the magnetic piece used in the PDMA process is removed from the inductor after the PDMA assembly. It is found that the presence of permalloy makes the position of the assembled inductor susceptible to external magnetic disturbance. Moreover, permalloy is believed to increase the series resistance of the spiral coil and degrade the inductor's quality factor due to its relatively low conductivity and high permeability [21], [22]. The high permeability of permalloy decreases the skin depth, which results in higher effective series resistance at the frequencies where the inductor may operate.

Third, in order to reduce current crowding in the spiral coil, we used circular spirals instead of rectangular ones, and increased the open space at the center of the spiral coil [23]–[25].

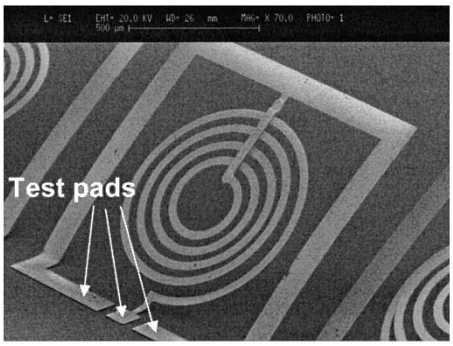
A schematic illustration of the fabrication process of the second-generation on-chip vertical spiral inductors is shown in Fig. 8. First, a 0.2-μm-thick aluminum film is deposited onto a substrate and patterned to serve as the first sacrificial layer [see Fig. 8(a)]. A 0.3-μm-thick copper layer is deposited, which is followed by the electroplating of 10-μm-thick copper layer [see Fig. 8(b)]. Second, a 10-μm-thick photoresist (AZ 4620) film is spun onto the substrate and baked to realize the dielectricspacer [see Fig. 8(c)]. Third, a 0.3-μm-thick copper layer is deposited, which is followed by the electroplating of a 10-μm-thick copper thin film [see Fig. 8(d)]. Next, the second sacrificial layer, a 10-μm-thick photoresist film (AZ 4620) is spun onto the substrate and baked to completely cover the electroplated copper coil structure. Finally, a 0.3-μm-thick copper layer is deposited to serve as the seed layer of a subsequent electroplating of a 20-μm-thick layer of Permalloy [see Fig. 8(e)].

After the fabrication, the first sacrificial layer is removed [see Fig. 8(f)] and the PDMA assembly is performed [see Fig. 8(g)]. The second sacrificial layer is then completely removed, allowing the permalloy piece to be detached from the copper inductor structure [see Fig. 8(h)].

Scanning electron micrographs of an on-chip spiral inductor (with nominal inductance of 10 nH) fabricated using the above process are shown in Fig. 9. In Fig. 9(a), the permalloy piece is intentionally removed to show the spiral inductor.



(a)



(b)

Fig. 9. Scanning electron micrographs of a second-generation on-chip spiral inductor. (a) Before the PDMA assembly. (b) After the PDMA assembly and removal of the permalloy piece.

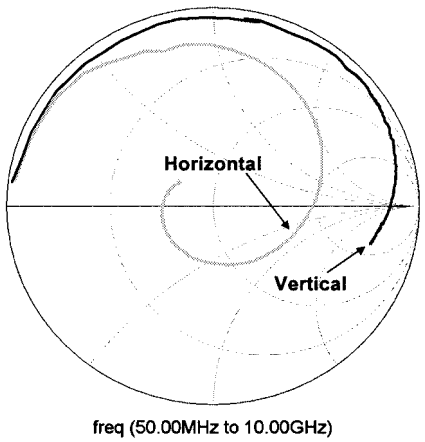


Fig. 10. Measured S_{11}-parameter (without deembedment) of the on-chip spiral inductor shown in Fig. 9(a) and (b).

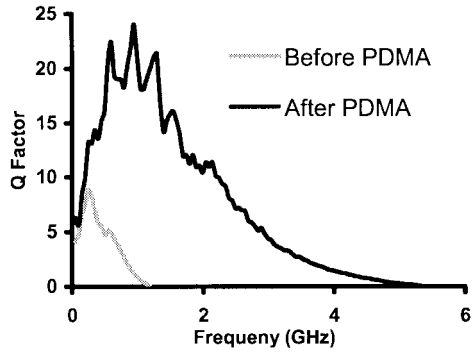


Fig. 11. Quality factor Q as a function of frequency extracted from the measured S_{11}-parameter results of the spiral inductor shown in Fig. 9(a) and (b).

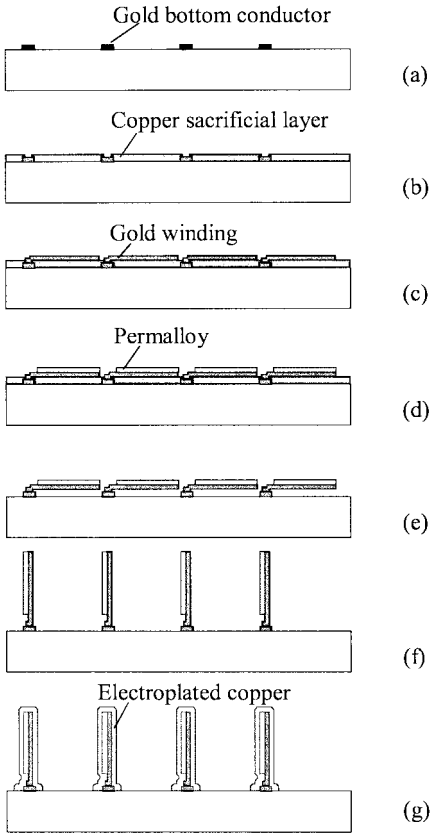


Fig. 12. Schematic diagram of the fabrication process of prototype on-chip solenoid inductors.

The S_{11}-parameter of the second-generation vertical spiral inductor is measured from 50 MHz to 10 GHz using an HP 8510C network analyzer and a Cascade coplanar GSG-150 probe. The measurement is made before and after the assembly for comparison. Fig. 10 shows the measured S_{11}-parameter results (without deembedment) of the spiral inductor shown in Fig. 9(a) and (b). The quality factor $\mathcal{Q}$ as a function of operation frequency is extracted from the measured S_{11}-parameter results using the same procedure discussed before (Fig. 11).

The second-generation inductors produce increased peak quality factor compared with the first-generation ones. When the spiral inductor is on the silicon substrate, it exhibits a peak quality factor of 8 and self-resonance frequency of 1.1 GHz. With the spiral inductor in the vertical position, the peak quality factor and the self-resonance frequency increase to 24 and 5.5 GHz, respectively.

It is conjectured that higher quality factor and self-resonance frequency can be achieved by further refining the design and fabrication process. However, this is beyond the scope of this paper, which serves to demonstrate the validity of the methodology.

IV. Development of On-Chip Solenoid Inductors

Prototype on-chip solenoid inductors have been successfully fabricated. In our process, gold is used as the material for both metal layers (Metal 1 and Metal 2), while copper serves as the sacrificial layer. This fabrication process can be realized on different substrates, such as semiconductor and glass (Fig. 12).

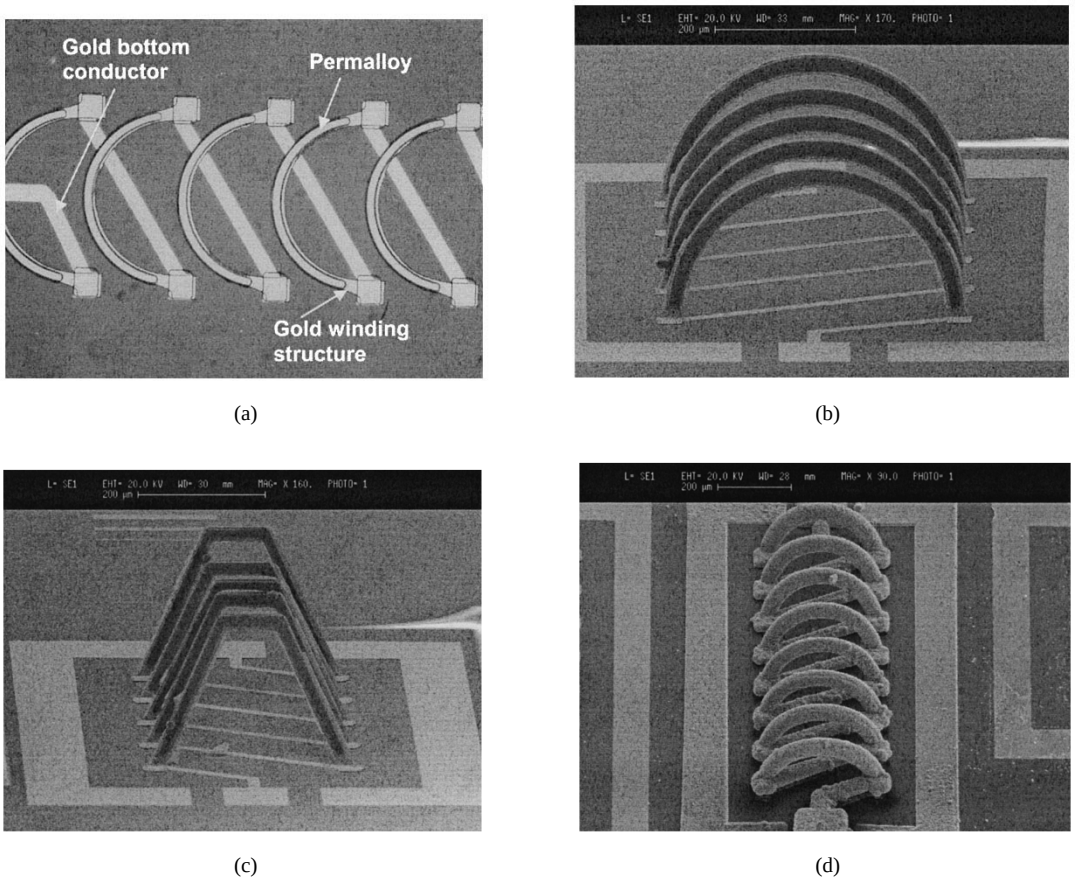


Fig. 13. Scanning electron micrographs of prototype on-chip solenoid inductors. (a) Before PDMA. (b) and (c) After PDMA. (d) After copper electroplating.

First, a 0.5-μm-thick gold thin film is evaporated onto the substrate and patterned to form bottom conductor (Metal 1) traces [see Fig. 12(a)]. Second, a 0.3-μm-thick copper is evaporated and patterned to serve as the sacrificial layer [see Fig. 12(b)]. Via-holes are formed by selectively removing the copper layer to expose the Metal-1 gold layer at the ends of all parallel lines. Third, a second gold layer (0.5-μm thick) is deposited and patterned to define the winding structure (Metal 2), shown in Fig. 12(c). The Metal-2 layer contacts the Metal-1 patterns at the via-holes. Next, permalloy material (5-μm thick) is electroplated onto the Metal-2 layer [see Fig. 12(d)]. Finally, the copper sacrificial layer [see Fig. 12(e)] is removed and the PDMA process is performed [see Fig. 12(f)]. We have demonstrated that it is possible to electroplate copper onto the Metal-1 and Metal-2 winding even after the PDMA assembly to further reduce the series resistance [see Fig. 12(g)].

Scanning electron micrographs of several fabricated prototype on-chip solenoid inductors are shown in Fig. 13. Fig. 13(a) shows the top view of a solenoid inductor before PDMA is performed, whereas Fig. 13(b) illustrates the same inductor after PDMA assembly. Fig. 13(c) shows a solenoid inductor with a unique cross section. Fig. 13(d) shows a solenoid inductor after copper electroplating.

Two-port S-parameter measurement of the fabricated prototype solenoid inductors has been conducted using two Cascade ground–signal–ground (GSG) 150 probes and an HP 8510C network analyzer from 50 MHz to 10 GHz. The measurement results of the solenoid inductor shown in Fig. 13(d) are shown in Fig. 14. The inductance value and the quality factor Q are extracted from the S-parameter measurement results without deembedding the probe contact pads (Fig. 15). A maximum Q of 10.5 at 1 GHz and an inductance value of 2.5 nH have been achieved. The inductance value can be further increases if the overall length of the inductor is extended.

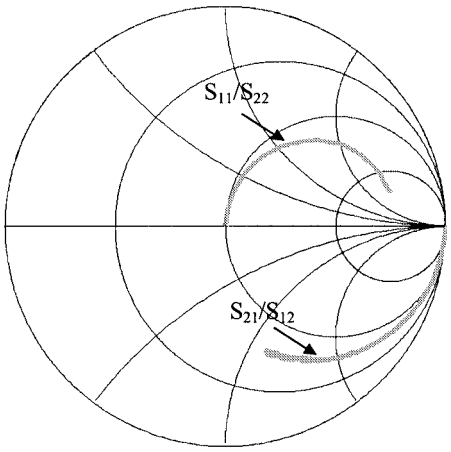
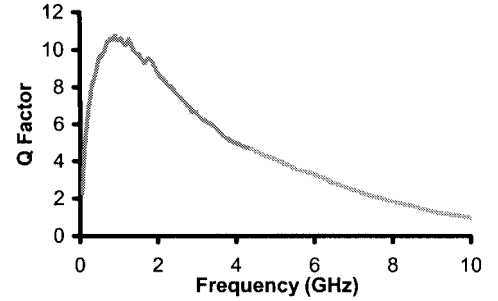


Fig. 14. Two-port S-parameter measurement results of the on-chip solenoid inductor shown in Fig. 13(d).



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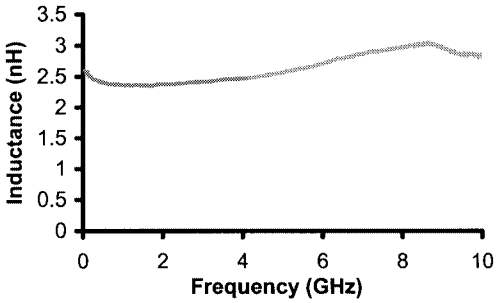

(b)

Fig. 15. Extracted inductance and the quality factor Q of the on-chip solenoid inductor shown in Fig. 13(d).

V. Discussion and Conclusion

Two types of on-chip 3-D inductors have been successfully developed using a novel and efficient 3-D assembly process, including vertical spiral inductors and solenoid inductors. The vertical spiral inductors are first fabricated on the substrate and then assembled into vertical position. Experimental results show that they exhibit higher quality factor and resonant frequency than their in-plane counterparts due to reduced substrate loss and parasitics. For the solenoid inductors, 2-D winding structures are first fabricated on the substrate and then assembled into vertical position to form a complete solenoid structure. On-chip solenoid inductors with different winding shapes and cross-sectional areas have been demonstrated for the first time. The fabrication processes proposed for both vertical spiral inductors and solenoid inductors are compatible with different substrates and current RFIC fabrication foundry.

Though the PDMA-based 3-D inductors have been presented in the context of RF circuit design, other applications exist or will be enabled by the proposed techniques, such as active control of power management devices within an IC. Integrated power electronic (dc–dc) converters have smaller size, higher reliability, faster dynamic response, and better energy efficiency [26]. However, the major limitation of integrated power converters has been the passive components, which occupy up to 90% of the total space of the converter and are very lossy at the high switching frequencies they operate [27]. If the PDMA-enabled 3-D inductors are applied, the power and space efficiency improvements will be substantial. The authors are currently pursuing a prototype of this concept.

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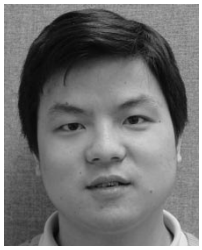

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